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Wide Range Time Difference Amplifier (WR-TDA)

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Abstract—This paper introduces a wide input range time difference amplifier (WR-TDA) with a linear, high amplification gain and low power consumption. A detailed analysis of the time amplification behavior is discussed. The effects of crucial design parameters such as load capacitance, supply voltage and key transistor parameters on amplification gain, linearity and input range were examined. Circuit simulations suggest that time amplifier can be tuned for wide input ranges with acceptable time gains. Moreover, gain linearity can be improved by properly optimizing a set of design parameters of the proposed circuit. This approach achieves an amplification gain up to 30ps/ps with a linear dynamic range of 10-1340ps and low power consumption. It also found that the biasing voltage (V_{bias}) significantly improves linearity of the amplification gain.

Keywords—Amplification Gain, Input range, Process variations, Time mode circuits, Time difference amplifier (TDA).

I. INTRODUCTION

Aggressive developments in CMOS technologies have primarily been driven by ever stringent market demands for low-cost, highly integrated, digital systems with very challenging performance requirements. However, as technology advances, analogue systems based on traditional design approaches, in particular voltage mode circuits, are required to cope with voltage headroom loss resulting from the dramatic reduction in supply voltage and the slow decline of threshold voltage of MOSFET devices [1]-[5]. Moreover, the reduced voltage headroom also deteriorates signal to noise ratio (S/N), increases nonlinearity effects in MOSFET devices and reduces input dynamic range of voltage based circuits [1], [6], [7]. As a result, they undermine the voltage accuracy levels of an analog system. The current-mode approach, on the other hand, provides an alternative path to circumvent voltage headroom loss and its effects on analog systems [1], [7], [8]; however, this approach suffers from the increased power consumptions due to the presence of low impedance nodes in such systems [7]. As a result, they are mainly employed in applications where speed rather than power is of the most critical concern. In general, the negative effects of voltage headroom loss on the performance of analogue circuits can be remunerated to an acceptable degree with help of digital means. This, however, comes at the cost of increased circuit complexity and high power consumption [1], [9].

In recent years, time-mode approaches have received much attention as they offer a means to overcome the seemingly unbeatable challenges in the analog designs because of their highly digital essence [1], [8]. In other words, time-mode approaches are capable of processing analog signals in the digital domain which renders them to advance from one technology generation to another with the minimum design time. Subsequently, they lower the cost and increase their ability to achieve analogue functionalities using digital structures [1], [10]. In this approach, information is represented with time variables in which a time difference between two pulses or two rising (or falling) edges is directly related to the magnitude of the analogue signal instead of representing them with an analogue nodal voltage or a branch

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current in analog designs [1], [4], [10]. Therefore, time mode approaches are capable of offering a technology-friendly means for data conversions and processing high-frequency analogue signals without using power-greedy and speed-impaired digital signal processors [11], [12]. Time-mode analog to digital converters (TADCs) with very high time resolution up to 9 bits, 1.08ps, low power consumption 0.667mW at a frequency of 200MHz, and a figure of merit (FOM), 0.0065pJ/conv, has been reported [6]. Similar to voltage amplifiers in analog systems, time difference amplifiers (TDAs) transform small time differences or duration between input signals into larger time differences or duration outputs. Therefore, they are considered one of the major building blocks in time mode designs. They are valuable for achieving high performance, especially speed, and resolution for the overall time domain processing system [1]. Time amplification is often needed in applications where the width of a narrow pulse is too small to be quantized accurately. Time amplifiers play a pivotal role in improving the resolution of time-mode circuits such as time arithmetic operators and time to digital or digital-to-time converters.

Recently, several types of time difference amplifiers (TDAs) have been reported. The authors of [13] implemented a time difference amplifier using the analog behavior in a regenerative bi-stable element and its time-responding characteristic in particular, the metastability phenomenon in a Set-Rest (SR) latch. A fundamental limitation of such an approach is that the time gain of the TDA is determined by the gain of the cross-coupled gates comprising SR latch. Consequently, this approach is sensitive to the effect of process, voltage and temperature (PVT) variations. Moreover, this type of time amplifiers provides a short input range and large gain variations [14], [15]. Several research works were conducted to address these challenges. For instance, the time difference amplifier proposed by Lee and Abidi enhances the input dynamic range of the time difference amplifier based on metastability by using two delay elements to generate an unbalanced re-generation mechanism [16]. However, time mismatch of the delay elements might be significant when input signals are too close to each other. This drawback can be removed by an adopting unbalanced active charge pump load as proposed in [17]. In an effort to reduce the level of PVT effects on TDA performance, delay locked loop (DLL) based time amplifier was firstly incorporated by Rashidzadeh *et al.* using a closed loop to program the gain of time amplification [18]. However, this approach requires that each TDA has a distinctive gain calibration technique. As a result, the deployment of this type of time amplifiers for high-speed applications is rather difficult [19]. A different approach of implementing TDA is proposed in [20]. This approach achieves an accurate amplification gain within an acceptable linear region by using the current source of the same polarity to achieve matching. However, additional active component and zero-crossing-detector are considered necessary. A pulse-train time amplifier is proposed in [11]. It is capable of realizing an accurate and digitally controlled TDA gain. However, this particular approach of TDA produces a pulse train rather than a single amplified pulse; and it could be only used with certain types of time digital converters (TDC) back ends. More recently, Molaei *et al.* proposed a technique employing current subtraction in place of the changing strength of current sources using conventional gain compensation methods, which result in a more stable gain than a wider input range [21]. Moreover, Wenlan Wu, *et al.* proposed a feedback time difference amplifier with a very high gain over a small input range and low power consumption [15]. The author of [22] has also proposed a novel 2× time-difference amplifier (TDA) with a small amplification gain over ±150ps input time-difference range and low standard variation of the gain under various process, voltage and temperature (PVT) conditions. This paper presents a wide-range TDA based on a current starved inverter with time resolution in a sub-picosecond range. The proposed WR-TDA achieves an acceptable

amplification gain with a very high degree of linearity. Moreover, the gain and dynamic measurement range of the proposed TDA can be adjusted by properly setting the width of the transistors along with other crucial parameters.

II. DESIGN OF TIME DIFFERENCE AMPLIFIER CIRCUIT

Time difference amplifiers (TDAs), as shown in Fig. 1, are mainly used to stretch and amplify time difference between two input signals. The input signals T_{in1} and T_{in2} are fed with the time delay between them as ΔT_{in}. The time difference between input signals and the output is ΔT_{out}.

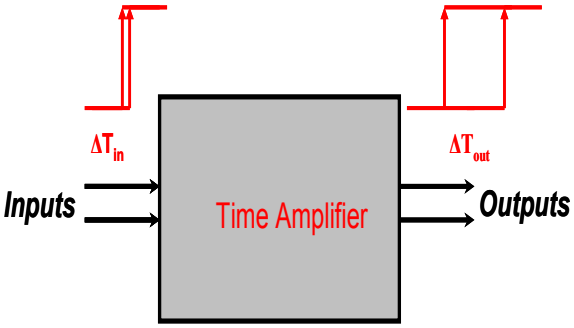

Fig. 1. A basic block diagram of a time difference amplifier (TDA)

Fig. 2 shows the CMOS implementation of the proposed time difference amplifier. In this approach, two input signals (T_{in1}) and (T_{in2}) are fed into the first building block which is composed of a pass transistor M_{n1} acting as a variable resistance. The transistor operates in a linear mode. The first stage is mainly used to convert the time difference between inputs into an output voltage which is directly related to the input time difference ($\Delta T_{in}=T_{in2}-T_{in1}$). Thereafter, the resulting output voltage is used to control the current flow in the second building block which is composed of a current starved delay element. The NMOS transistor M_{n3} is also used to add a degree of freedom to control the delay of the proposed TDA with the help of a biasing voltage. The transistors M_{p1} and M_{n4} constitute a current mirror circuit which is used to control the charging and discharging currents of the output capacitance of the first inverter by varying gate voltages of transistors M_{p2} and M_{n5}. The second stage inverter is used for improving the rise and fall times of the circuit. Sometimes, multiple cascaded inverters could be used for this purpose. The transistors M_{p1}, M_{n4}, M_{p2} and M_{n5} operate in a saturation mode in order to source/sink currents in the starved delay element. By controlling the charging/discharging current of the output parasitic capacitor (C_{out}), it is feasible to modulate the propagation delay of this element. This in turn transfers the input time difference into a larger delay time at the output terminal; and the result of this operation is ΔT_{out}. It is also worth to notice that the time amplification action of the proposed TDA circuit is not based on the metastability phenomenon which could occur in the feedback inverter. Those inverters cloud be replaced by a single inverter which is mainly used to regenerate/reshape the output voltage of the pass transistor. In summary, the modification of the standard current starved delay element was related to the addition of the transistor M_{n1} and the feedback inverters that act as a nonlinear time to the voltage converter. The drain currents of MOSFETs M_{n4} and M_{p1} are set by the resultant control voltage. Currents in M_{n4} and M_{p1} are mirrored in each source/sink transistors of the starved inverters M_{P2} and M_{n5}, respectively. Consequently, this modification helps reduce the nonlinear delay variation and greatly improve the quality of the performance of the standard current starved delay element at the expense of the small area overhead.

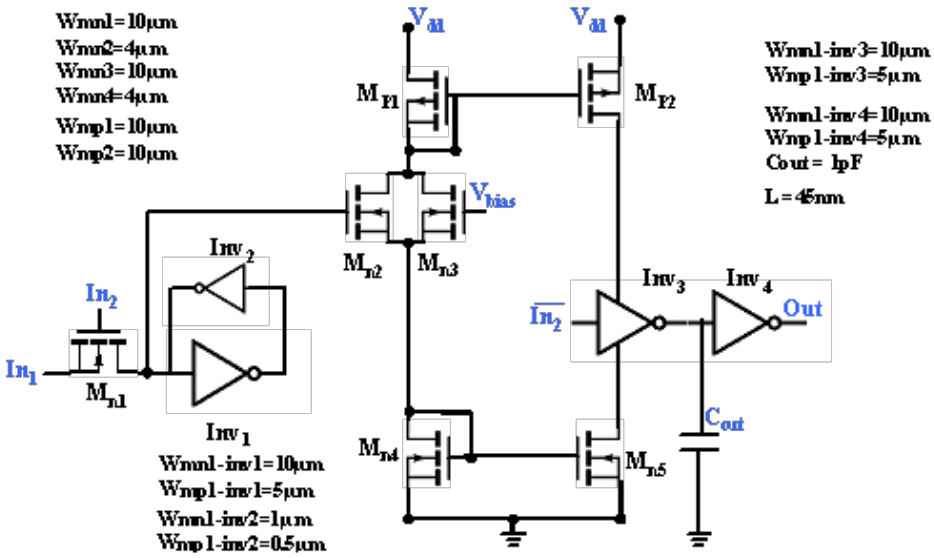

Fig. 2. CMOS implementation of the proposed WR-TDA circuit

Fig. 3 illustrates the relationship between the delays obtained from the current starved delay element and control voltage. A single element delay can span from minimum to infinite gate delay. This curve is obtained with the help of HSPICE circuit simulation for transistor models of 45nm standard CMOS technology node [23] with supply voltage V_{dd}=0.9V. As shown in Fig. 3, the range of delay variation is large but non-linear; and is analytically defined as follows [24]

$$T_{delay} = \frac{C_{out}}{\frac{k_n}{2}.\frac{W}{L}.(V_{control} - V_{th}).\lambda} \ln\left(\frac{1+\lambda V_{dd}}{1+\lambda \frac{V_{dd}}{2}}\right) \quad (1)$$

where C_{out} is output load capacitance; V_{dd} is supply voltage; K_n is the technology parameter; λ is the channel length modulation parameter; W/L is the aspect ratio of the control transistor; V_{th} is threshold voltage; and $V_{Control}$ is control voltage which, in this paper, is directly related to the time difference of input signals.

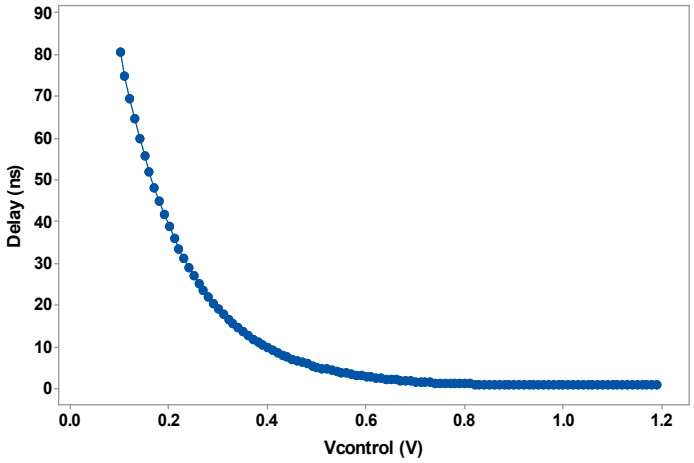

Fig. 3. The transfer curve (Delay-Control voltage) of the current starved delay element

To demonstrate the ability of the proposed TDA to amplify the time difference of the two input signals, circuit simulations were undertaken using 45nm model card [23] with a single supply voltage V_{dd}=0.9V. Fig. 4 shows the TDA waveforms of output (V_{out}) for different input time intervals ranging from -300ps to 300ps.

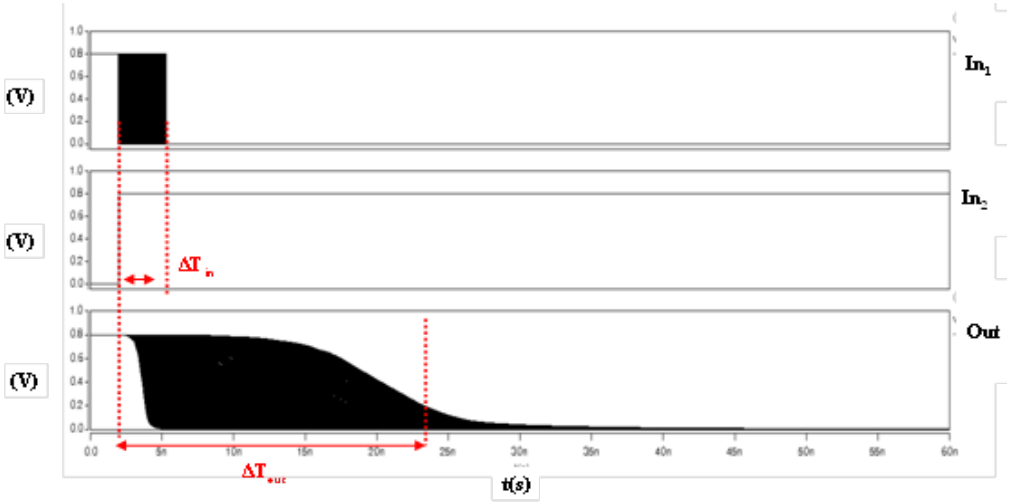

Fig. 4. Output transient waveforms of the proposed time amplifier for different input time intervals

A typical transfer curve (ΔT_{out}-ΔT_{in}) for TDA circuit, which is shown in Fig. 5, demonstrates the amplification of the proposed TDA and its ability to maintain a fairly linear conversion behavior for a very wide input range time difference. However, for larger time differences, the transfer characteristic becomes non-linear and saturated; it signifies some range limitations of the proposed circuit.

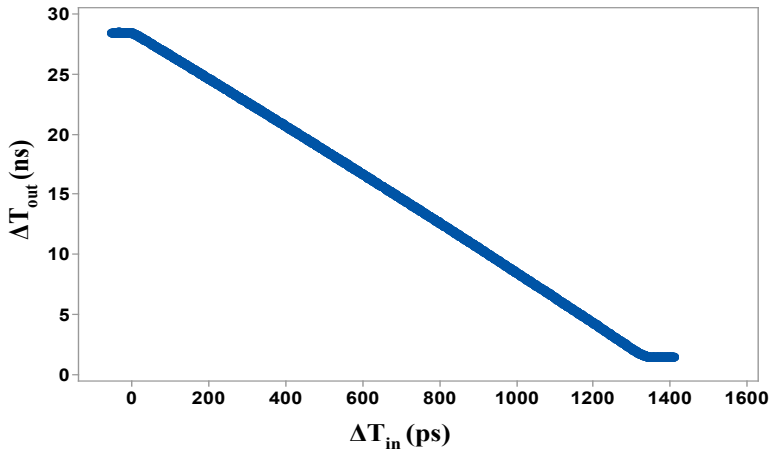

Fig. 5. Transfer curve (ΔT_{out}-ΔT_{in}) of the proposed TDA

The amplified time difference at the output (ΔT_{out}) denotes as the time difference between the output signal and the input signal (T_{in2}). The input-output relationship of the proposed time amplifier for a small (ΔT_{in}) within the dynamic range is defined as ΔT_{out}=A ΔT_{in}, where A is denoted as the time amplifier gain coefficient and is equal to the slope of the transfer curve in Fig. 5. It can be seen from (1) that the power supply, threshold voltage and aspect ratios of the transistors are vital factors in setting the gain of the time amplifier proposed. Furthermore, a large gain can be obtained by cascading more TDA stages.

III. RESULTS AND DISCUSSION

Circuit simulations were undertaken with help of the HSPICE circuit simulator and Minitab statistical tool to illustrate the effects of various design parameters on the performance of the TDA proposed. The design parameters that are considered in this work are mainly supply voltage (V_{dd}), biasing voltage (V_{bias}), threshold voltage of both NMOS and PMOS devices (V_{thn} and V_{thp} respectively), load capacitance (C_{out}) and transistor widths (W_n and W_p). Fig. 6 demonstrates the effect of the supply voltage (V_{dd}) and basing voltage (V_{bias}) on the amplification gain of the TDA proposed. It can be seen that when utilising higher supply voltages and lower biasing voltages, it is possible to achieve higher amplification gains. This can be explained due to the direct relationship between power supply voltage (V_{dd}) and the average time constant of the system (T_{delay}), as evident in (1). The delay obtained is inversely proportional to variations in basing voltage (V_{bias}).

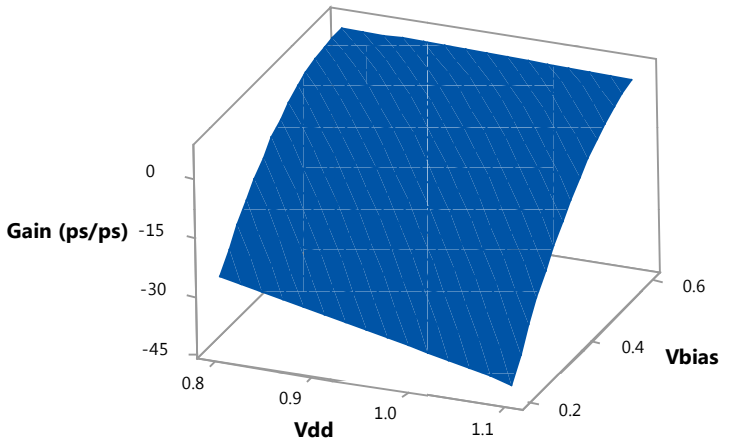

Fig. 6. The influence of Vdd and Vbias on gain of time amplifier

The effect of the threshold voltages of both NMOS and PMOS devices is shown in Fig. 7. It is evident that using higher threshold voltages for transistors can possibly achieve larger time amplification gains. On the other hand, using larger PMOS devices in term of channel width of transistors can also provide higher time gains of the proposed circuit as illustrated in Fig. 8. This might be explained by the fact that the current strength of the PMOS devices noticeably increases as the device width increases; and hence the rate at which the total charge is delivered to the output capacitance is increased. This consequently increases the gain of the time amplifier. A slight impact on the time amplification gain can be also noticed when varying the output capacitance as demonstrated in Fig. 9.

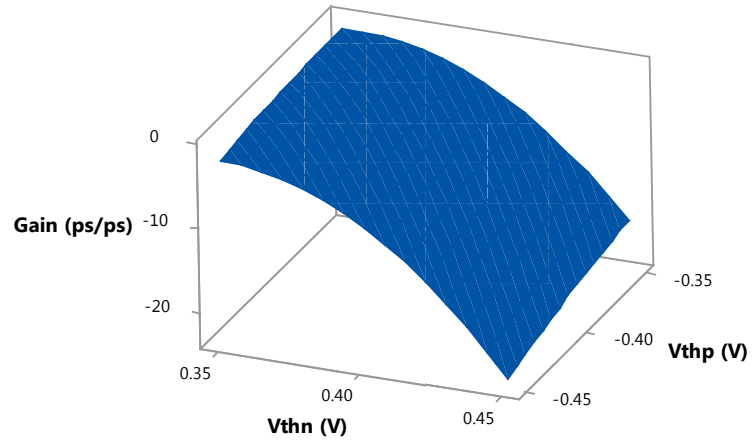

Fig. 7. The influence of Vthn and Vthp on gain of time amplifier

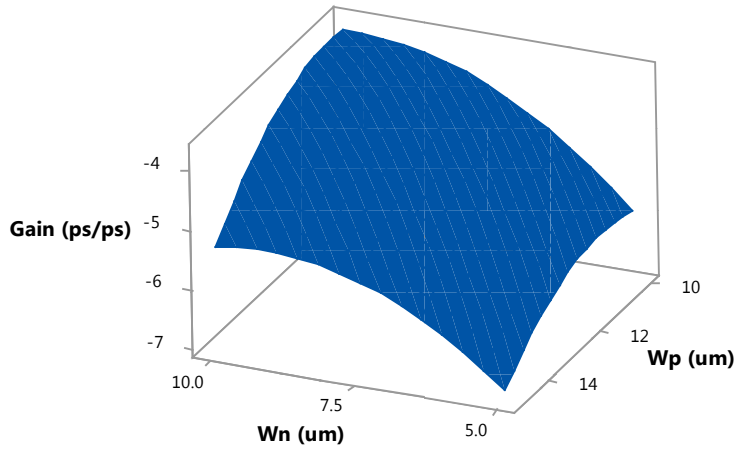

Fig. 8. The influence of Wn and Wp on gain of time amplifier

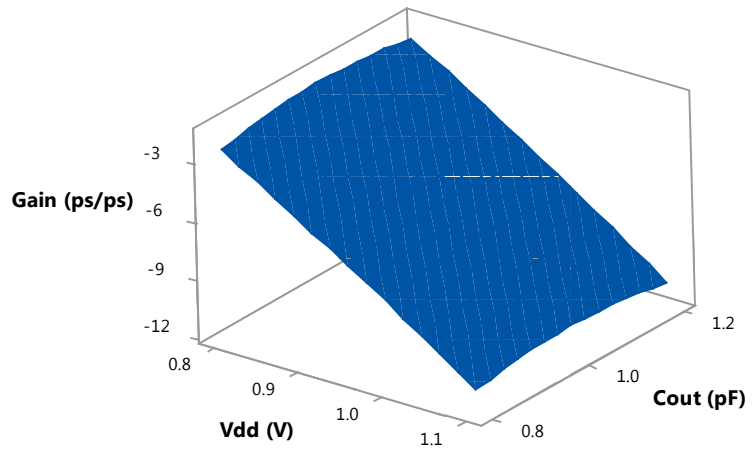

Fig. 9. The influence of Vdd and Cout on gain of time amplifier

Fig. 10 shows a histogram plot of the gain variations of the proposed TDA for different input intervals. The nominal value of the gain of the proposed circuit is found to be 4ps/ps; and the standard deviation of the gain is 0.51ps/ps.

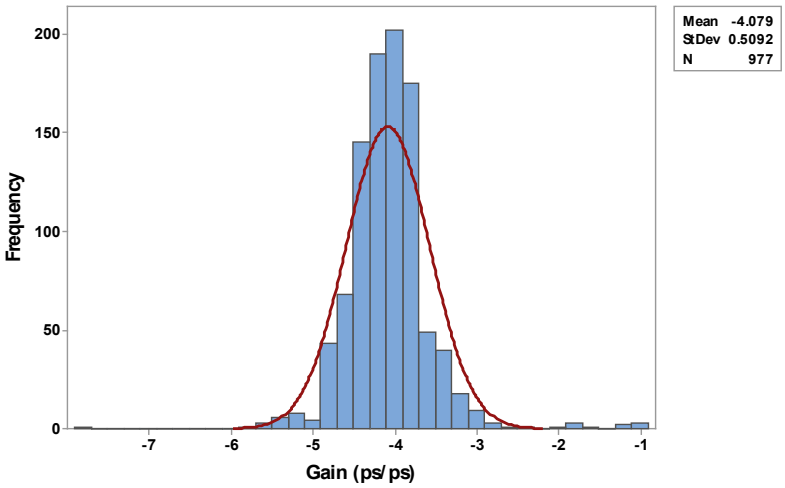

Fig. 10. Histogram plot of the gain variations of a time amplifier for different time intervals

Fig. 11 demonstrates the effect of the supply voltage V_{dd} and basing voltage (V_{bias}) on the standard deviations of the gain for different input time intervals which represent gain linearity over the input range. It can be seen that using lower power supply voltages can achieve less variations in the amplification gain while using higher biasing voltages (V_{bias}) significantly reduce amplification gain errors for different time intervals of the proposed time amplifier. Moreover, using larger device widths could reduce deviation from the mean values and improve gain linearity of the proposed time amplifier as demonstrated in Fig. 12. Moreover, using lower threshold voltages devices can also reduce time amplification variations. A slight impact can be noticed on gain variations when changing the output capacitance as shown in Fig. 13.

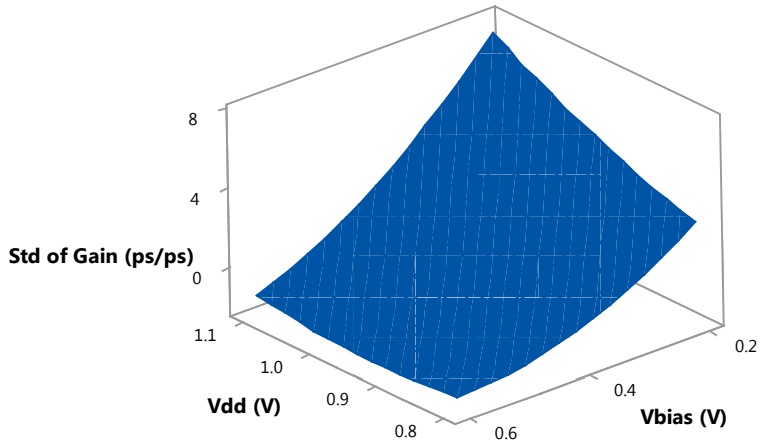

Fig. 11. The effect of Vdd and Vbias on standard deviation of time amplifier gain

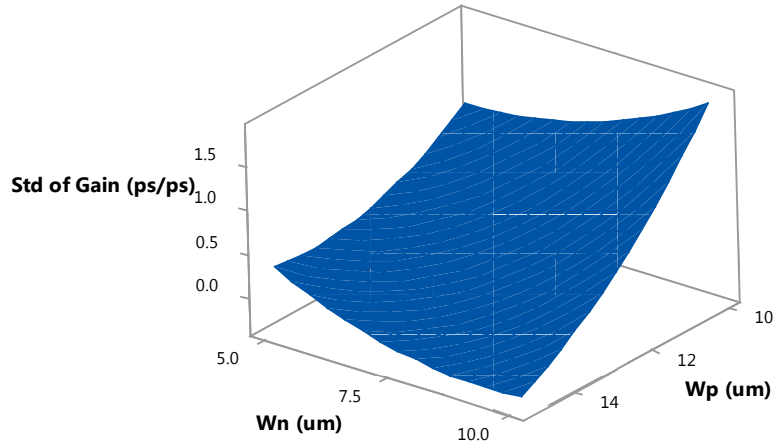

Fig. 12. The influence of transistors width on the standard deviation of the time amplifier gain

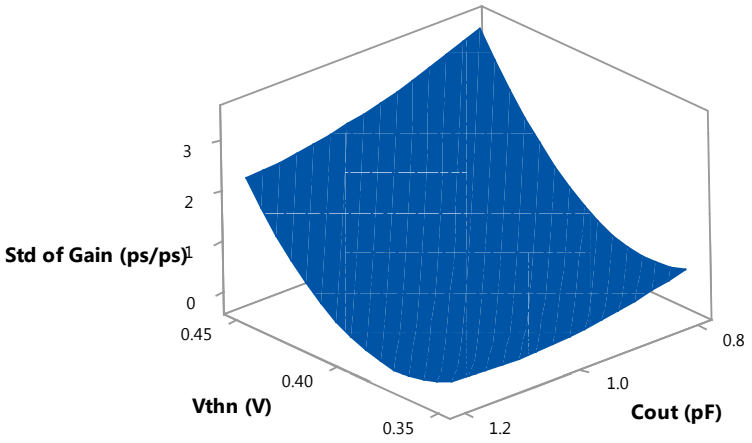

Fig. 13. The influence of Cout and Vthn on the standard deviation of the time amplifier gain

Fig. 14 demonstrates the effect of the supply voltage and basing voltage on the input dynamic range of the proposed time difference amplifier. It can be seen that using lower power supply voltages can achieve a higher dynamic range. Using biasing voltages (V_{bias}) has a slight impact on the amplification dynamic range; using larger widths of PMOS devices increases the input range of the proposed TDA. Moreover, using smaller widths of both NMOS and PMOS devices increases the input range of the proposed TDA as shown in Fig. 15. Furthermore, it can be seen that using higher threshold voltages increases the input range of time amplification as demonstrated in Fig. 16. Similarly, it can be noticed that using large capacitance values at the output could enhance the input range of the time amplification process as shown in Fig. 17.

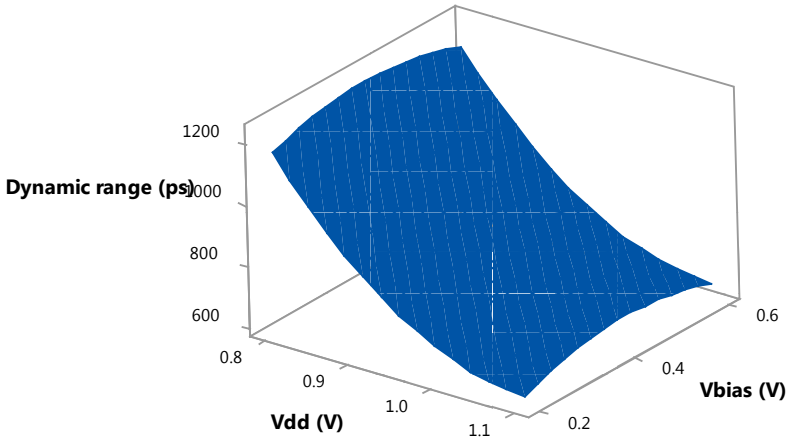

Fig. 14. The influence of Vdd and Vbias on input dynamic range of the proposed time amplifier

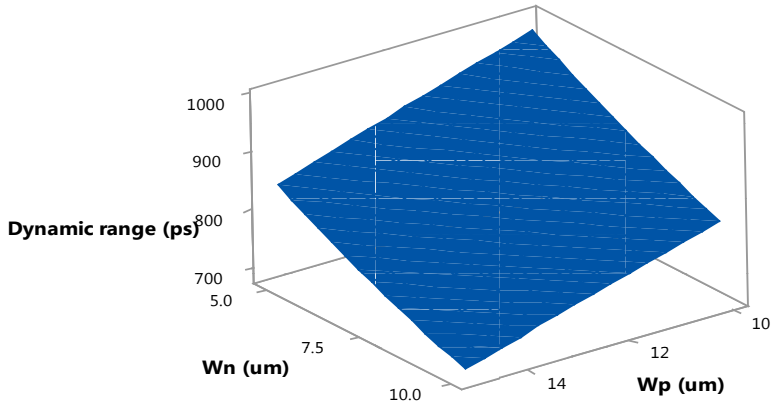

Fig. 15. The influence of Wn and Wp on input dynamic range of the proposed time amplifier

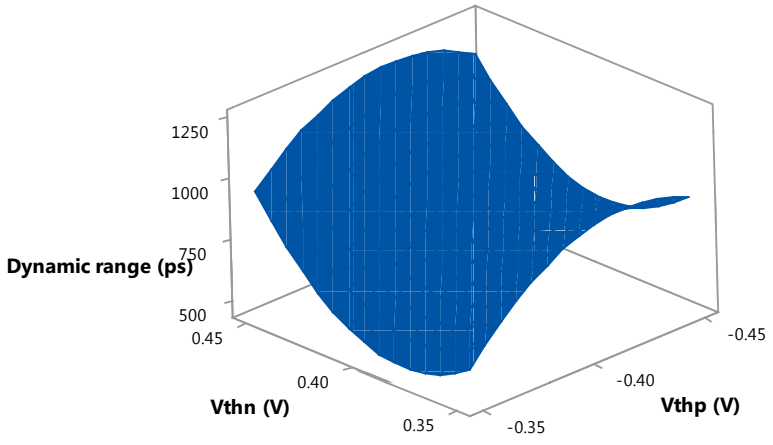

Fig. 16. The influence of Vthn and Vthp on input dynamic range of the proposed time amplifier

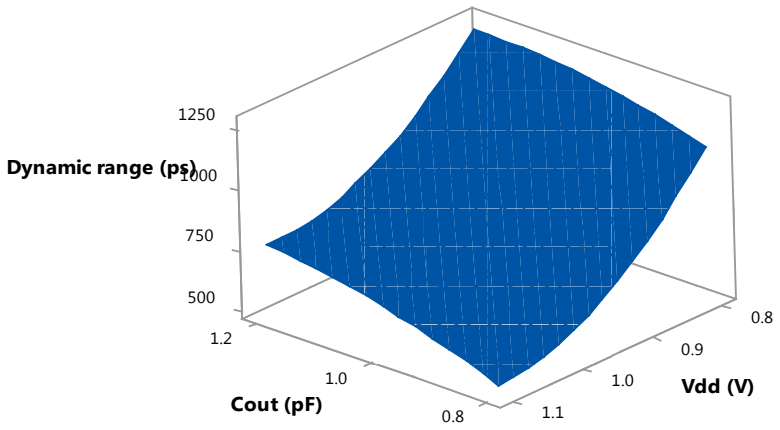

Fig. 17. The influence of Vdd and Cout on input dynamic range of the proposed time amplifier

By comparing the results of recently reported time amplifiers (TDAs) in terms of their overall performance, as tabulated in Table 1, it can be seen that RS-latch time amplifiers enjoy superior time resolution and low power consumption but suffer from a small input range. In particular , the TDA proposed by Heo *et al.* achieves an amplification gain up to 150 with a linear dynamic range of ±20ps and low power consumption [13]. On the other hand, DDL-based time amplifiers offer a large input range and a large gain but suffer from a speed penalty and a large silicon area overhead [18], [19]. More recently, Wenlan Wu. *et al* proposed a feedback time difference amplifier with a very high gain (25-734) over a small input range (±20 ps) using a 130nm technology node and power consumption 91.54µW for the highest gain [15]. Furthermore, Molaei *et al.* proposed a technique which employs current subtraction in place of changing the strength of current sources using conventional gain compensation methods, which result in a more stable gain over a wider input range that can be expanded up to 300ps [21]. The author of [22] has also proposed a novel 2×time-difference amplifier (TDA) in 65nm CMOS technology, where the TDA gain ranges from 1.99 to 2.02 over ±150ps input time-difference range; and the standard variation of the gain is 0.02 under various process variations. The simulated average of power consumption was 62µW. In this work, it was found that the input range of the proposed TDA is a range from 10-1340ps with a time amplification gain larger 30 times. Moreover, it provides a resolution time in the sub-picoseconds domain while consuming much lower power (122µW). Furthermore, the gain linearity can be improved using the biasing voltage along with other design parameters.

TABLE 1
PERFORMANCE COMPARISON OF RECENT TIME AMPLIFIERS BASED ON DIFFERENT APPROACHES

Reference	Technology Node	Gain	Dynamic Range, ps	Power, µW
[13]	110	27-150	±20	608
[15]	130	25-734	±20	91.54
[17]	90	4-17	16-480	--
[22]	65	1.99-2.02	10-200	62
[21]	180	2	300	28
This Work	45	30	10-1340	122

IV. CONCLUSIONS

A wide input range time difference amplifier (WR-TDA) with a linear and high amplification gain and low power consumption is presented. The WR-TDA transfer curves were obtained for crucial design parameters such as supply voltage, biasing voltage, load capacitor and transistor widths. The simulation results suggest that the amplification gain, gain variations

and input measurement range can be tuned by properly setting the width of the transistors in the proposed circuit along with other vital parameters. It also found that the biasing voltage (V_{bias}) significantly improves linearity of the amplification gain in the proposed time amplifier. Additionally, a large gain can be obtained by cascading more TDA stages.

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